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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,836	08/21/2003	SZETSEN STEVEN LEE	11088-US-PA	1835

31561 7590 07/13/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,836	LEE, SZETSEN STEVEN	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 8 is objected to because of the following informalities: "over temperature" apparently should be -- over heating --. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Sasaki et al. (U.S. Patent No. 6,796,269).

5. As to claim 1, Sasaki discloses a detecting method for a dry etching machine, comprising: perform an etching process on a preset number of wafers (column 4, lines 44-55), wherein Vpp values with respect to the wafers are recorded in the etching

process (column 6, lines 25-30; Figure 5B); obtaining a Vpp range under a working condition, according to the Vpp values of the wafers (column 6, lines 41-67); feeding the Vpp range to a control system of the dry etching machine; and comparing Vpp values for a subsequent wafer under the etching process (column 7, lines 24-30), wherein when the Vpp values are out of the Vpp range, then the control system of the dry etching machine enters an abnormal operation mode (column 7, lines 32-47).

6. As to claim 2, Sasaki discloses that the preset number of the wafers is equal to or greater than 200 (Figure 5B).

7. As to claim 3, Sasaki discloses that the Vpp range is determined according to a mathematical analyzing algorithm (column 7, lines 24-30).

8. As to claim 4, Sasaki discloses that when the etching machine enters the abnormal operation mode, the control system stops the etching machine (column 7, lines 32-47).

9. As to claim 5, Sasaki discloses that when the etching machine enters the abnormal operation mode, the control system issues a warning signal (column 7, lines 32-47).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki.

12. As to claim 10, Sasaki does not expressly disclose a situation that the Vpp values are out of the Vpp range caused by the abnormal oxygen flowing rate. However, Sasaki discloses that the normal value of voltage amplitude Vpp (column 6, lines 66-67; column 7, lines 1-4) must first be obtained for a variety of predetermined etching conditions (column 6, lines 50-56; Figure 7) before monitoring abnormal plasma discharge (column 6, lines 60-65). Sasaki further discloses etching with oxygen gas at a predetermined flow rate and mixture ratio (column 4, lines 53-55). Moreover, abnormal plasma discharge may result in a large number of poorly processed wafers (column 8, lines 26-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a situation that the Vpp values are out of the Vpp range caused by the abnormal oxygen flowing rate. One who is skilled in the art would be motivated to terminate the etching of the wafer once an abnormal plasma discharge is detected, including abnormalities caused by an improper oxygen flow rate.

13. Claims 6-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki, in view of Wolf et al., *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press (1986) ("Wolf I").

14. As to claim 6, Sasaki does not expressly disclose a situation that the Vpp values are out of the Vpp range caused by the pad layer, with thermal conducting but electrical insulation, on an E-chuck (ESC) being broken. However, Sasaki discloses that the normal value of voltage amplitude Vpp (column 6, lines 66-67; column 7, lines 1-4) must

first be obtained for a variety of predetermined etching conditions (column 6, lines 50-56; Figure 7) before monitoring abnormal plasma discharge (column 6, lines 60-65). Moreover, abnormal plasma discharge may result in a large number of poorly processed wafers (column 8, lines 26-37). Wolf I teaches that a large number of parameters affect the etching process (pages 546-47), including the temperature of the wafer surface (Figure 5, page 546). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a situation that the Vpp values are out of the Vpp range caused by the pad layer, with thermal conducting but electrical insulation, on an E-chuck (ESC) being broken. One who is skilled in the art would be motivated to terminate the etching of the wafer once an abnormal plasma discharge is detected, including abnormalities caused by an improper wafer temperature.

15. As to claim 7, Sasaki does not expressly disclose a situation that the Vpp values are out of the Vpp range due to helium leakage, which is used to chill the wafers, caused by breakage of the transport pipe of internal helium gas in the E-chuck (ESC). However, Sasaki discloses that the normal value of voltage amplitude Vpp (column 6, lines 66-67; column 7, lines 1-4) must first be obtained for a variety of predetermined etching conditions (column 6, lines 50-56; Figure 7) before monitoring abnormal plasma discharge (column 6, lines 60-65). Moreover, abnormal plasma discharge may result in a large number of poorly processed wafers (column 8, lines 26-37). Wolf I teaches that a large number of parameters affect the etching process (pages 546-47), including the temperature of the wafer surface (Figure 5, page 546). Therefore, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to include a situation that the Vpp values are out of the Vpp range due to helium leakage, which is used to chill the wafers, caused by breakage of the transport pipe of internal helium gas in the E-chuck (ESC). One who is skilled in the art would be motivated to terminate the etching of the wafer once an abnormal plasma discharge is detected, including abnormalities caused by an improper wafer temperature.

16. As to claim 8, Sasaki does not expressly disclose a situation that the Vpp values are out of the Vpp range due to over heating on the bottom of the etched wafer. However, Sasaki discloses that the normal value of voltage amplitude Vpp (column 6, lines 66-67; column 7, lines 1-4) must first be obtained for a variety of predetermined etching conditions (column 6, lines 50-56; Figure 7) before monitoring abnormal plasma discharge (column 6, lines 60-65). Moreover, abnormal plasma discharge may result in a large number of poorly processed wafers (column 8, lines 26-37). Wolf I teaches that a large number of parameters affect the etching process (pages 546-47), including the temperature of the wafer surface (Figure 5, page 546). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a situation that the Vpp values are out of the Vpp range due to over heating on the bottom of the etched wafer. One who is skilled in the art would be motivated to terminate the etching of the wafer once an abnormal plasma discharge is detected, including abnormalities caused by an improper wafer temperature.

17. As to claim 9, Sasaki does not expressly disclose a situation that the Vpp values are out of the Vpp range caused by insufficient performance of a chilling system.

However, Sasaki discloses that the normal value of voltage amplitude Vpp (column 6, lines 66-67; column 7, lines 1-4) must first be obtained for a variety of predetermined etching conditions (column 6, lines 50-56; Figure 7) before monitoring abnormal plasma discharge (column 6, lines 60-65). Moreover, abnormal plasma discharge may result in a large number of poorly processed wafers (column 8, lines 26-37). Wolf I teaches that a large number of parameters affect the etching process (pages 546-47), including the temperature of the wafer surface (Figure 5, page 546). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a situation that the Vpp values are out of the Vpp range caused by insufficient performance of a chilling system. One who is skilled in the art would be motivated to terminate the etching of the wafer once an abnormal plasma discharge is detected, including abnormalities caused by an improper wafer temperature.

18. As to claim 11, Sasaki does not expressly disclose a situation that the Vpp values are out of the Vpp range is caused by a defect of the etched wafer itself. However, Sasaki discloses that the normal value of voltage amplitude Vpp (column 6, lines 66-67; column 7, lines 1-4) must first be obtained for a variety of predetermined etching conditions (column 6, lines 50-56; Figure 7) before monitoring abnormal plasma discharge (column 6, lines 60-65). Moreover, abnormal plasma discharge may result in a large number of poorly processed wafers (column 8, lines 26-37). Wolf I teaches that a large number of parameters affect the etching process (pages 546-47), including the temperature of the wafer surface (Figure 5, page 546). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a

situation that the Vpp values are out of the Vpp range is caused by a defect of the etched wafer itself. One who is skilled in the art would be motivated to terminate the etching of the wafer once an abnormal plasma discharge is detected, including abnormalities caused by surface effects.

19. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki, in view of Wolf, *Silicon Processing for the VLSI Era*, Vol. 2, Lattice Press (1992) ("Wolf II").

20. As to claim 12, Sasaki does not expressly disclose that the dry etching machine is used in a deep trench process for dynamic random access memory (DT-DRAM). Wolf II teaches that deep trench structures are used to serve as a storage capacitor structure from DRAM devices (page 51), which are commonly used as a memory device (page 570). Moreover, dry etching is used to form characteristics such as, smooth and slightly tapered sidewalls, smooth and rounded bottom corners, and uniform depth (pages 51-52). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dry etching machine in a deep trench process for dynamic random access memory (DT-DRAM). One who is skilled in the art would use dry etching to achieve desirable trench characteristics to fabricate a DRAM, a commonly used semiconductor memory device.

21. As to claim 13, Wolf II discloses that the deep trench process uses a reaction ion etching process (DT-RIE) (pages 51-52).

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kosugi (U.S. Patent No. 6,197,116) discloses an etch chamber with a sensor for measuring electrical signals from the plasma. Kagoshima et al. (U.S. Patent No. 6,733,618) discloses a system for monitoring a plasma during semiconductor etching.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER

EBC
July 6, 2005